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Methodology for the Computer-Aided Design of Silicon Micromachined Devices in a Standard CMOS Process

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Abstract

The methodology for implementing the design of silicon micromachined devices in a standard CMOS foundry process is discussed, and a modified Magic technology file is introduced. The modified technology file is used to design silicon micromachined devices and circuits that are fabricated using a standard CMOS foundry through the MOSIS service. An additional maskless etch in EDP is required to realize the micromechanical structures once chips are delivered. The modified technology file implements a layer that we call "open" that consists of a combination of active area, contact cut, via, and glass opening. This open area exposes the silicon surface for the anisotropic etch procedure that creates suspended bridges of polysilicon or metal encapsulated in SiO_2. Results from fabricated chips are included.

Key words: CAD; CIF; CMOS; EDP etch; micromachining; MOSIS; open area; pixel; technology file.

1. Introduction

The recently successful use of commercial standard CMOS foundries for the fabrication of silicon micromachined devices [1-4] suggests the need for high-level computer-aided design (CAD) software such as Magic[1] [5,6] for device design and integration with digital or analog electronics. A CIF (Caltech Intermediate Form) or calma file can be generated using Magic which contains the mask-specific digitized data. This file can be sent to MOSIS. Many benefits can be derived from using standard foundry processes such as those available through the MOSIS service [7] to manufacture these structures. The benefits include low cost, high yield, and easy integration of digital and analog electronics with the reliability of a standard process automatically built into the circuit. Furthermore, the use of standard foundries makes silicon micromachining possible for universities, government laboratories, and businesses that do not have an in-house custom integrated circuit (IC) fabrication facility.

In this paper, the Magic technology file is used to build transducer devices in the form of pixels. Most of the smart microelectronic transducers reported to date consist of substrate electronics with one or more additional specialized layers of polysilicon, piezoelectric, or pyroelectric material. The substrate electronics implements the drive and control functions, and the additional layer(s) are used to produce the transducer function. The transducer function of the additional layer(s) is based on its material properties. The concept of integrating the transducer device on the same substrate as the drive and control electronics (as opposed to the mechanical attachment of transducer devices to the IC electronics or separate electronic and transducer devices) is highly desirable and leads to lower cost systems when produced in high volume. This is equivalent to the savings realized from VLSI circuits as opposed to the expensive equivalent printed circuit (PC) boards of discrete devices. This concept is generally referred to as integration and the integrated transducers with the substrate electronics are referred to as smart transducers [8].

In general, when manufacturing smart transducers the circuitry is fabricated first using a standard IC fabrication process. After the circuits are fabricated, additional post-processing steps are performed to realize the transducers. Additional specialized layers of polysilicon, piezoelectric, or pyroelectric material can be deposited and etched, and silicon micromachining can also be done. These post-processing steps usually create suspended structures like diaphragms or cantilevers by the removal of a sacrificial material [9] or by the silicon micromachining of a portion of the silicon substrate [10,11]. These additional steps are usually custom in nature and require specialized processing tools.

In order to design these structures in large systems, the use of high-level CAD software is necessary to reduce the level of complexity and to save design time. In this work, a design

---

[1] Certain commercial equipment, instruments, and computer programs are identified in this paper to specify the procedure adequately. This does not imply recommendation or endorsement by NIST, nor does it imply that the equipment or program is the best available for the purpose.

methodology is presented that was incorporated into the current SCMOS technology file for Magic to implement the fabrication of silicon micromachined device structures. This technology file uses only the layers supplied by a commercial standard CMOS process. Higher level CAD editors now available need modifications for the automated design of these devices. Technology files for Magic contain technology-specific information such as mask layers, design rules, etc. In order to incorporate a new layer that we call "open," which opens up or exposes the appropriate area for the anisotropic etch, the technology file had to be modified. It is this modification of the SCMOS technology file which makes micromachining through MOSIS possible.

The main advantage of this technique is that no major equipment is needed and the post-processing is reduced to a single maskless etch step. The main disadvantage is that custom layers are not incorporated in the design; therefore, the sensors/transducers are composed of polysilicon and/or aluminum sandwiched with thermal oxide and CVD oxide, available in the commercial CMOS process, which form suspended structures. These structures have a very low thermal mass and can be heated to incandescence with low power. The structures have already been demonstrated for use as a gas flow sensor [2] and as an infrared (IR) point source [3].

2. Description of the Magic Technology File

The Magic technology file [5,6] is composed of sections each starting with a keyword and ending with the word "end" as shown below:

"section keyword"
.
.
.
end

A listing of some of the Magic section "keywords" used in this paper are shown in table 1 along with a brief description as to their purpose. Each section of a technology file consists of a series of lines, and each line consists of a series of words separated by spaces.

Table 1. Magic Section "Keywords" With Brief Description

Section Keyword	*Description*
tech	technology file name
planes	listing of the planes
types	listing of the tiles associated with which planes
contact	contacts between planes
styles	colors associated with the tiles
compose	to create structures in the same plane
cifoutput	to output a CIF or calma file
cifinput	to read in a CIF or calma file
drc	design rule checker

The "tech" section defines the technology to be used and the "planes" section specifies the names of the planes to be used. The "types" section identifies the technology-specific tiles used by Magic and the plane on which they reside. Each tile can be categorized as a primary layer, an interconnection between layers, or a transistor. No two tiles on the same plane can reside on the same digitized space. If this is attempted, either a new tile is created, or the previous tile is erased. Each line in the "types" section is in the form of "*plane names(tiles).*"

The "styles" section lists all the tiles along with the color-coded numbers used to make up each tile on the CAD system. The "cifoutput" section describes how to generate mask layers from Magic's abstract layers. The mask layers are indicated by the CIF names which have three capital letters starting with the letter C denoting CMOS. The following two letters specify the intended mask. In the "cifoutput" section, the CIF names are followed by the Magic tile names to be included on the mask associated with the CIF name. Magic can generate CIF files as well as calma files, but we will concentrate our attention on the CIF attributes of Magic. The "cifinput" section defines the operation(s) needed to rebuild a Magic file from a CIF file of digitized mask data. Each Magic tile is specified first followed by a combination of CIF layers. The "drc" section specifies the design rules, for example, the width and spacing rules for the various tiles.

3. Specific Changes to the Technology File to Include Micromachining

In order to modify Magic's technology file to design micromachined silicon devices using a standard CMOS process, a new tile and plane called "open" is defined. The appendix shows the main features of the SCMOS technology file with the addition of the new tile "open," and the new plane also called "open." This tile makes micromachining through MOSIS possible. The modified "tech" section calls the new technology file "scm" (an abbreviation for scalable CMOS micromachine). In the "planes" section, the new plane called "open" is added resulting in a total of seven planes, some of which are referred to by more than one name. The scm technology file lists 23 tiles in the "types" section, each residing on one of the seven planes. In the "styles" section, a new line is added to include the new CAD color code for the tile open.

In the "cifoutput" section, the open area is specified on four different masks. Whenever the open area is digitized on the CAD system and when CIFed, the digitized area will be included on the active area mask (CAA), the contact mask (CCA), the via mask (CVA), and the glass mask (COG). These are the mask steps which during the fabrication process will expose the silicon surface. In practice after the chips are received from the foundry, through MOSIS, the suspended, machined devices are realized by an additional maskless etch in EDP (ethylene diamine-pyrocatechol-water[2]). The etch solution reacts with the exposed silicon surface defined by the digitized open areas while the SiO_2 acts as a mask. Additional details can be found in the references [10,11].

---

[2] In this work, the EDP etchant was purchased premixed from the Transene Company, Inc., part number PSE-300.

In the "cifinput" section, the layer "open" is defined as any tile containing the four digitized areas of active area (CAA), contact (CCA), via (CVA), and glass (COG).

The "drc" section specifies the design rules for the "open" to "open" minimum spacing between distinct structures to be 20 μm (assuming the chips are manufactured on a processing run where the feature size is 2.0 μm which generally corresponds to a lambda of 1). If this design rule is violated, these structures may become connected after the etch. The minimum size of the open area has not yet been determined. However, 5 μm (assuming a lambda of 1) has been used in a test structure, similar to the one described in the examples section below, to help determine the etch rate of the etchant. It may be difficult to obtain tighter processing control on the glass layer, a component of the open layer.

4. Design Considerations for Realizing Suspended Structures

To design layouts that realize suspended structures when standard CMOS chips are post-processed in an anisotropic etch, there are several design considerations. They include the alignment of the design and the use of p^+ boron doping to minimize undercutting. In this section, a brief overview of these considerations is presented, along with examples of a single cavity and multiple cavities which create the suspended structures. Some physical explanations are included; however, more detailed treatments can be found in the references [10-12].

The etchant used in this work, EDP, was chosen because both SiO_2 and Al can be used as masking materials. This is important since the surface of CMOS chips are covered by SiO_2 for passivation while the bond pads are aluminum. Therefore, the only areas exposed to the etch are the *open* regions designed in the CAD layout. These factors give rise to a maskless etch procedure for realizing the suspended structures in standard CMOS.

The first consideration involves the orientation and alignment of the design. In order to maintain control over the directions of the etch, designs must be aligned to lines which correspond to the intersection of the {111} crystalograghic plane (see ref. [13] for more details) and the wafer surface plane. This is easily accomplished if one designs structures on the Cartesian coordinate grid system, i.e., structures that are bounded by a perimeter that follows the x-y axis. The reason for this is that standard CMOS foundries use (100) silicon wafers for their process. The wafers are purchased with a *flat* that is oriented along this (110) intersection. The chips are aligned with respect to this wafer *flat*.

For example, figure 1 shows the case of a rectangular opening in the SiO_2 that is aligned to the x-y grid system of the CAD layout. Initially, figure 1a, the opening exposes the Si surface. After some intermediate time in the anisotropic etch, a pit is formed with a flat bottom, figure 1b. The side walls of the pit are bounded by the {111} planes and form a 54.74° angle with respect to the silicon surface plane. The material being etched is primarily at the bottom of the pit. After some final time, figure 1c, the four side walls intersect at a point, halting further etching.

The side walls of the pit form a 54.74° angle with the surface because the etch rate of the

etchant varies with the direction in the silicon crystal lattice, hence, the term anisotropic etch. Of primary importance is the fact that the etch rate is significantly slower in the <111> direction as compared to the <100> direction. The approximate ratio for the etchant used in this work for these two directions is 1:35 [11]. Therefore, the {111} planes can virtually be used as etch stops. Note that there is some undercutting of the Si-SiO_2 surface, shown in figure 1c, because the etch rate is not completely negligible in the {111} direction. This undercutting can be minimized by using a p^+ boron implant at the perimeter of the open area. This p^+ implant can be included in the design and provided by the foundry.

Figure 2 demonstrates the effect of misalignment of rectangular open area(s) to the x-y grid system. The open area in this case is rotated by 45° from the x-y grid. For a single pit as shown in figure 2a, after sufficient time in the etch solution, the etched pit will be formed by the smallest rectangle aligned to the x-y grid that encompasses the open region. For the case of two misaligned open areas that have intersecting pit regions, if formed individually, the pit area becomes the smallest rectangular area formed by the two openings combined, as shown in figure 2b.

Figures 3, 4, and 5 demonstrate the effects of multiple aligned openings. In figure 3, the openings are isolated and aligned. This leads to isolated pit regions. If these openings are now brought together, as shown in figure 4, the pit is defined by the largest rectangle formed by the openings. Note that this design realizes a suspended corner region. In the standard foundry process, this suspended structure can contain layer(s) of polysilicon and aluminum[3] encapsulated in glass. Finally, figure 5 demonstrates the design of a cantilever structure formed by a "U" shaped opening. In this paper, the pixel structure shown in figure 6 is used.

5. Design Examples Using Magic

Figure 7 is a test structure which includes the open tile. The open tile is the interior square which is surrounded by p^+ implant. This test structure is an aid in determining the etch rate of the etchant. This is done by observing the change in depth versus time of the open area for various sizes of structures similar to that shown in figure 7. The side walls in the open areas in the smaller structures will meet first thus halting the rapid etch. Once this depth is achieved, the etching occurs at a much slower pace where undercutting can occur. It has been shown that the p^+ implant reduces the undercutting [14]. This technique has been demonstrated in both n-well and p-well processes through MOSIS.

The CIF file for the digitized test structure in figure 7 that was created by the "scm" technology file was generated. This CIF file is given in table 2. Note that MOSIS's familiar SCMOS CIF layers are being used for the open tile.

Figure 8 shows the design of a pixel structure that is used as an infrared point source. This design was sent to MOSIS for fabrication as a 2.0-μm design. When the chips were

[3] The standard foundry process may have multiple layers of polysilicon and aluminum.

received from MOSIS, they were first dipped in a 2% buffered HCL solution for 10 s to strip away any native oxide in the open areas. The chips were then emersed in an agitated EDP solution at 100°C in a reflux container for $2\frac{1}{2}$ hours. This is the step that creates the suspended structures. The actual time spent in the EDP solution is a function of the device size. In general, one would like to minimize the time in the etch solution. A photomicrograph of the pixel taken after the etch is shown in figure 9.

Table 2. CIF File for the Test Structure in Figure 7

```
DS 1 1 2;
9 open50;
L CAA;
     B 22000 4000 -202600 4000;
     B 4000 14000 -211600 -5000;
     B 10000 10000 -202600 -5000;
     B 4000 14000 -193600 -5000;
     B 22000 4000 -202600 -14000;
L CVA;
     B 10000 10000 -202600 -5000;
L CCA;
     B 10000 10000 -202600 -5000;
L CSP;
     B 22800 4800 -202600 4000;
     B 4800 13200 -211600 -5000;
     B 4800 13200 -193600 -5000;
     B 22800 4800 -202600 -14000;
L COG;
     B 10000 10000 -202600 -5000;
DF;
C 1;
End
```

For the thermally isolated resistor shown in figure 9, incandescence was achieved with 10 V applied across the resistor and 10 mA yielding a low power of 100 mW. Incandescence is achieved at such low power because heat is not absorbed by the underlying silicon substrate. Figure 10 is a picture of the device operating at incandescence. The radiative intensity is controllable by the drive current as shown in figure 11. This device has possible applications in the area of dynamic thermal scene simulation [15].

6. Conclusions

A new technology file has been created by modifying the existing SCMOS Magic technology file available from MOSIS to include the feature "open." The incorporation of this feature makes it possible to realize suspended structures. If a resistor is suspended, it will glow given a voltage drop across it. This principle is now being applied to chips submitted as 2.0-μm designs to MOSIS. We are proposing this be the SCM technology with MOSIS, which is not the standard SCE submission. The relatively low cost, high yield, and reliability of design and fabrication using the MOSIS service makes silicon micromachining possible for

universities, government laboratories, and businesses.

This work was done for a lambda of 1 and further studies will need to be done for smaller feature sizes. On-going work for design of silicon micromachined structures in standard CMOS foundries includes further testing for development of optimum design rules including the minimum/maximum open size, the open-to-open spacing for separate structures and in the same structure to realize suspended structures, and the proximity of digital circuits. On-going work also includes studies yielding an optimized design of supports for suspension and an optimized device structure for thermal effects. Also, work in the development of standard libraries for micromachined devices in standard CMOS processes will be needed as more applications are developed. Testing and characterization measurements will also be required. Finally, more detailed understanding and modeling of the anisotropic etching of silicon as shown in ref. [16] are needed.

7. Acknowledgments

The authors would like to thank Wes Hansford and Vance Tyree from MOSIS for support in this work and Don Novotny at NIST for help with the post-process etching procedure. We also acknowledge the support from the Navy Advance Test Equipment/Metrology (ATE/M) Project at NOSC in San Diego, California, and the Army Test Measurements and Diagnostic Equipment (TMDE) Activity at Redstone Arsenal, Alabama.

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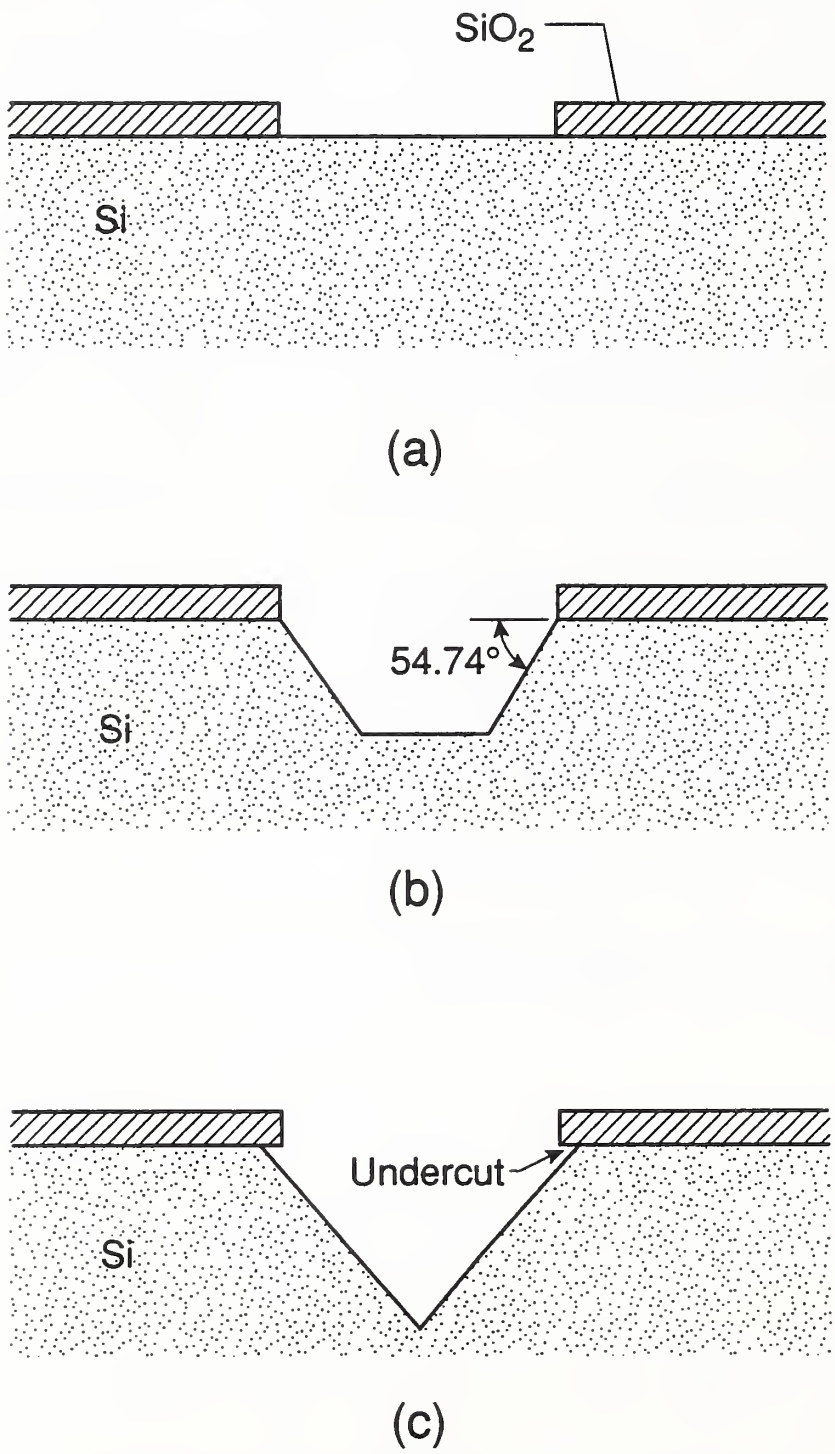
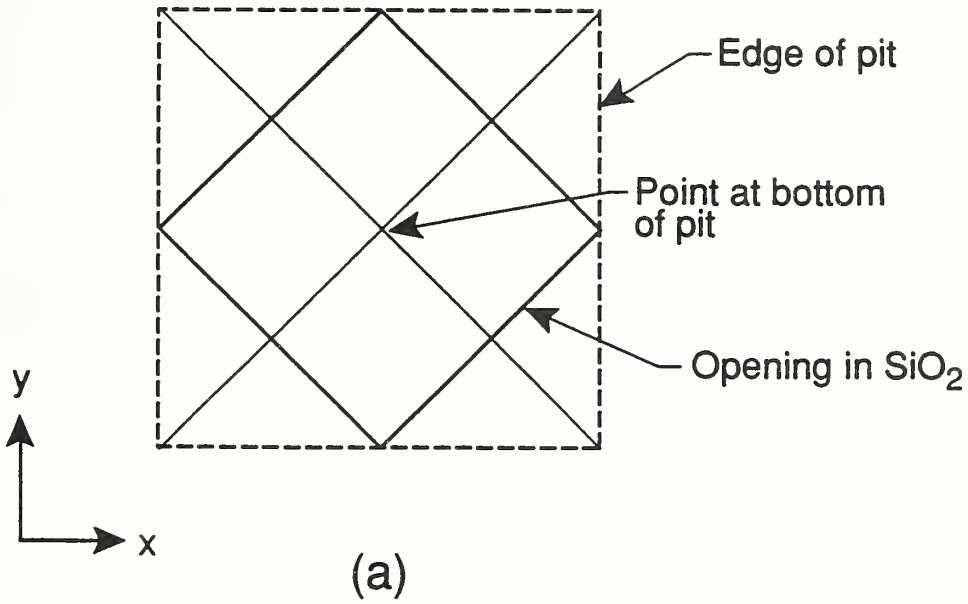


Figure 1. A cross-sectional view of the effects to the exposed silicon substrate due to the etchant (a) before the etchant is used, (b) at an intermediate stage, and (c) when the etching has stopped.



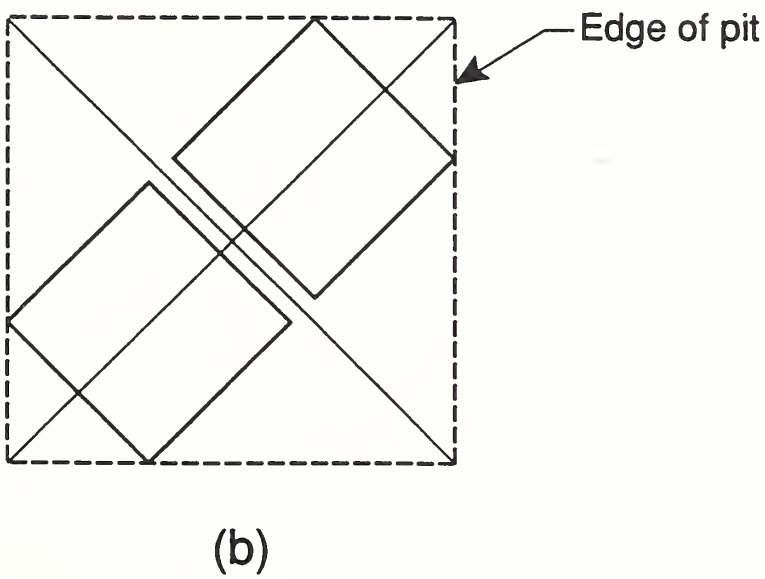


Figure 2. When the open areas are misaligned with the x-y grid system (a) for a single opening, the etched pit will be formed by the smallest rectangle aligned to the x-y grid that encompasses the open region, and (b) for two open areas with intersecting pit regions, the etched pit becomes the smallest rectangular area formed by the two openings combined.

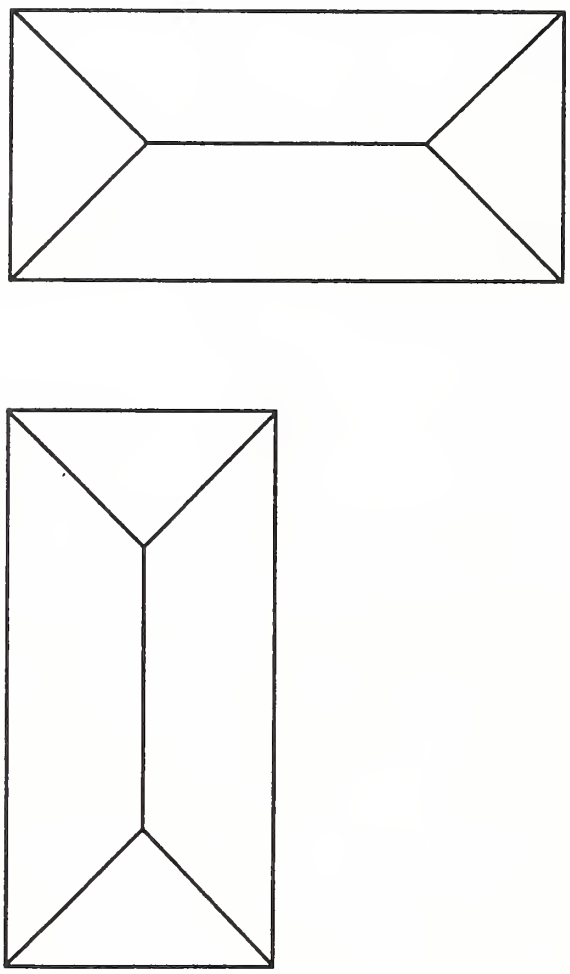


Figure 3. A top view of two openings that are isolated and aligned with the x-y grid.

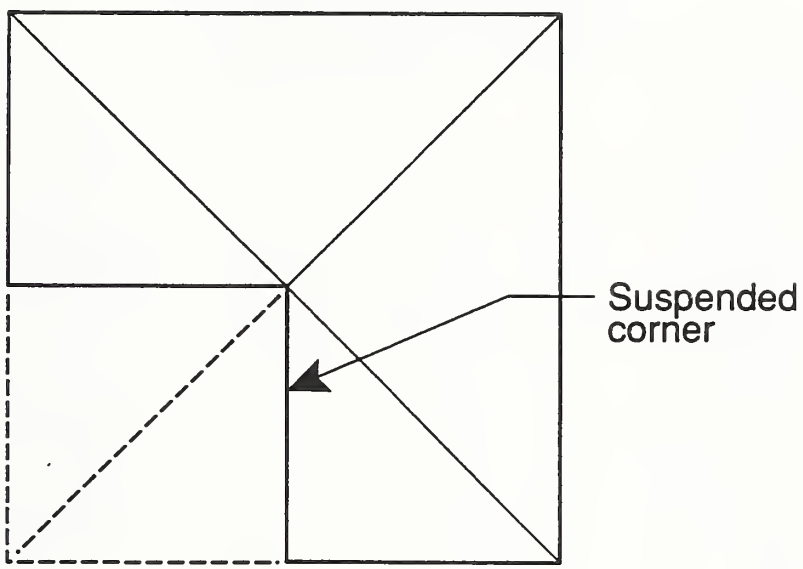


Figure 4. A top view of two openings similar to those shown in figure 3 however they are closer together. The pit is the largest rectangle formed by these openings and a suspended corner region results.

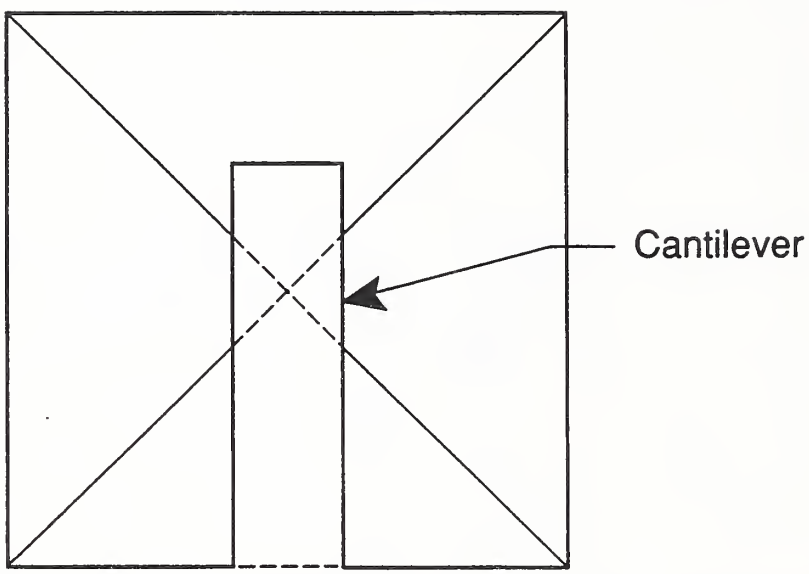


Figure 5. A top view of three rectangular openings in the shape of a "U." The pit is formed and a cantilever structure results.

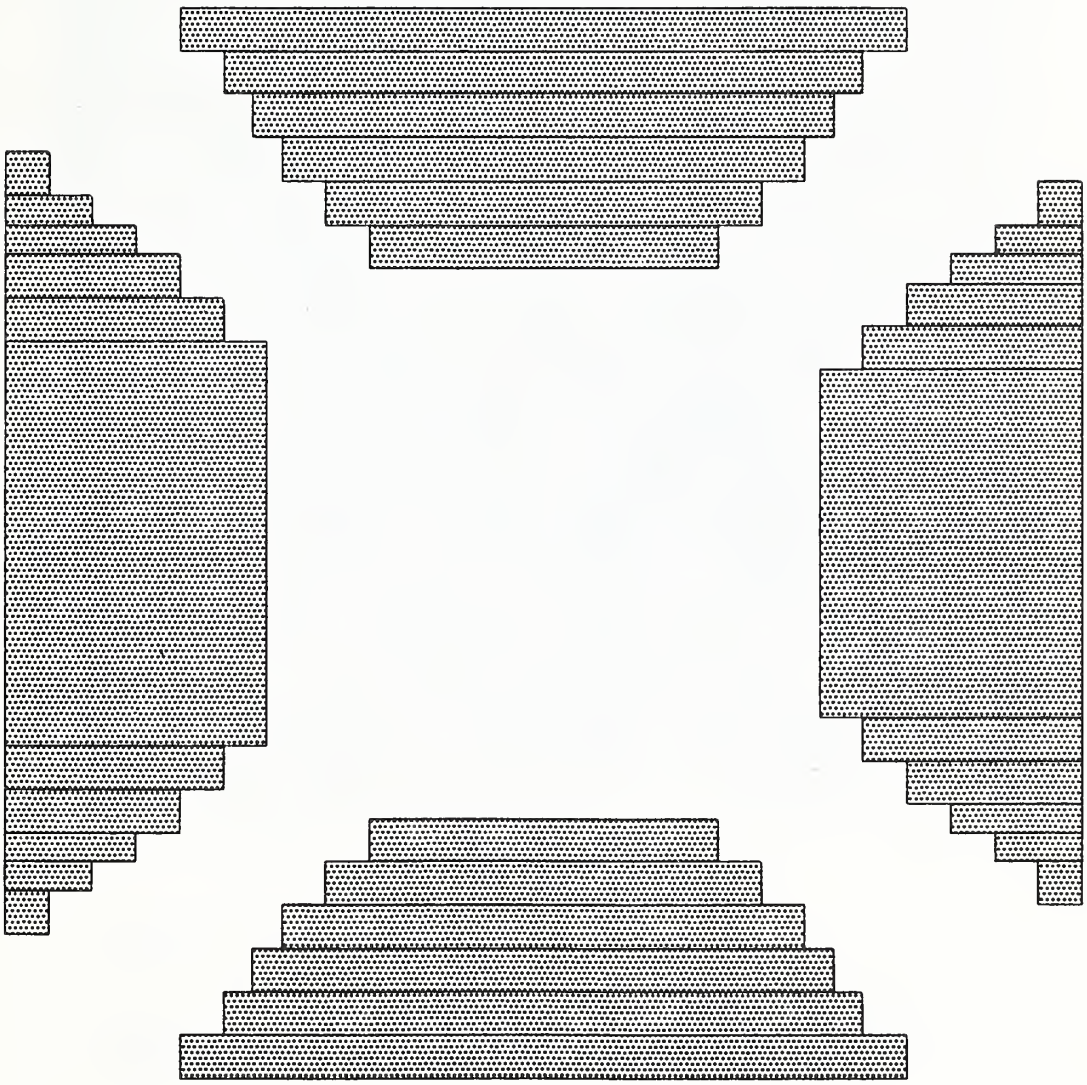


Figure 6. The openings used for the pixel structure.

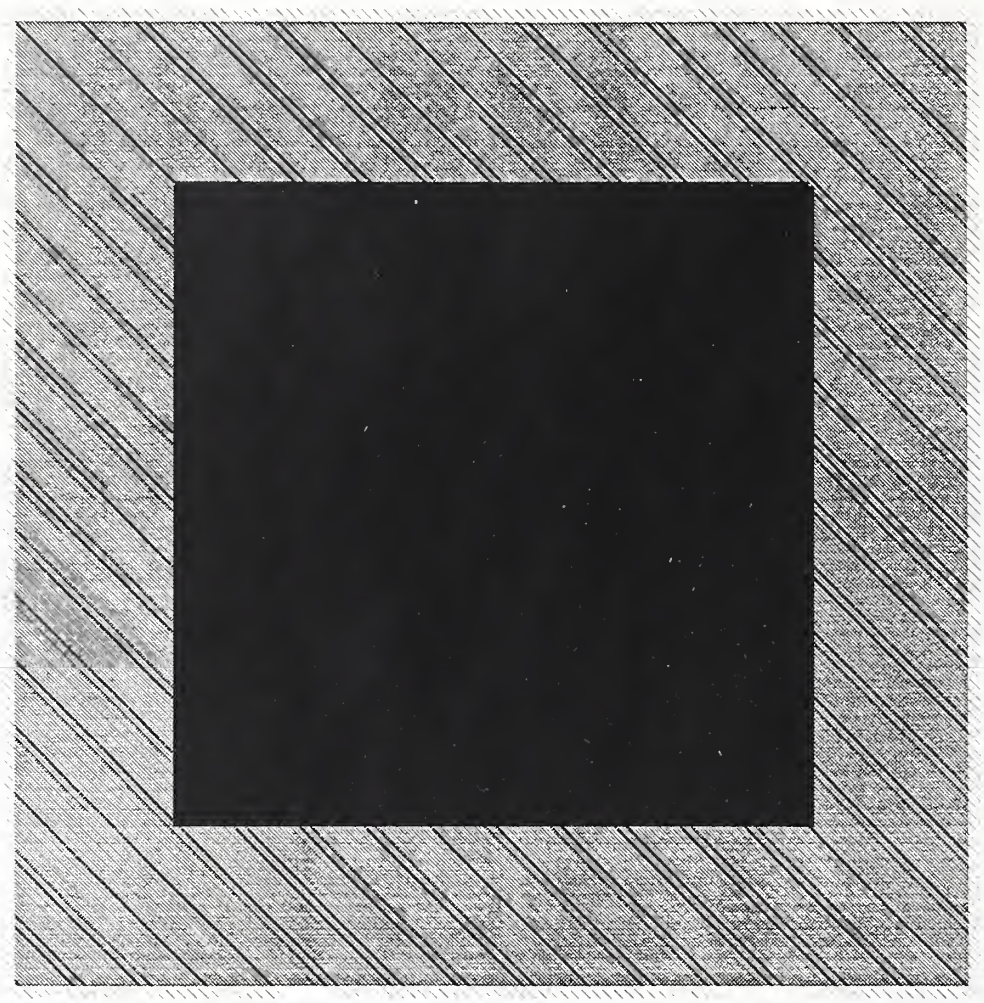


Figure 7. A test structure which includes the open tile with a surrounding p+ implant. This structure helps determine the etch rate of the etchant.

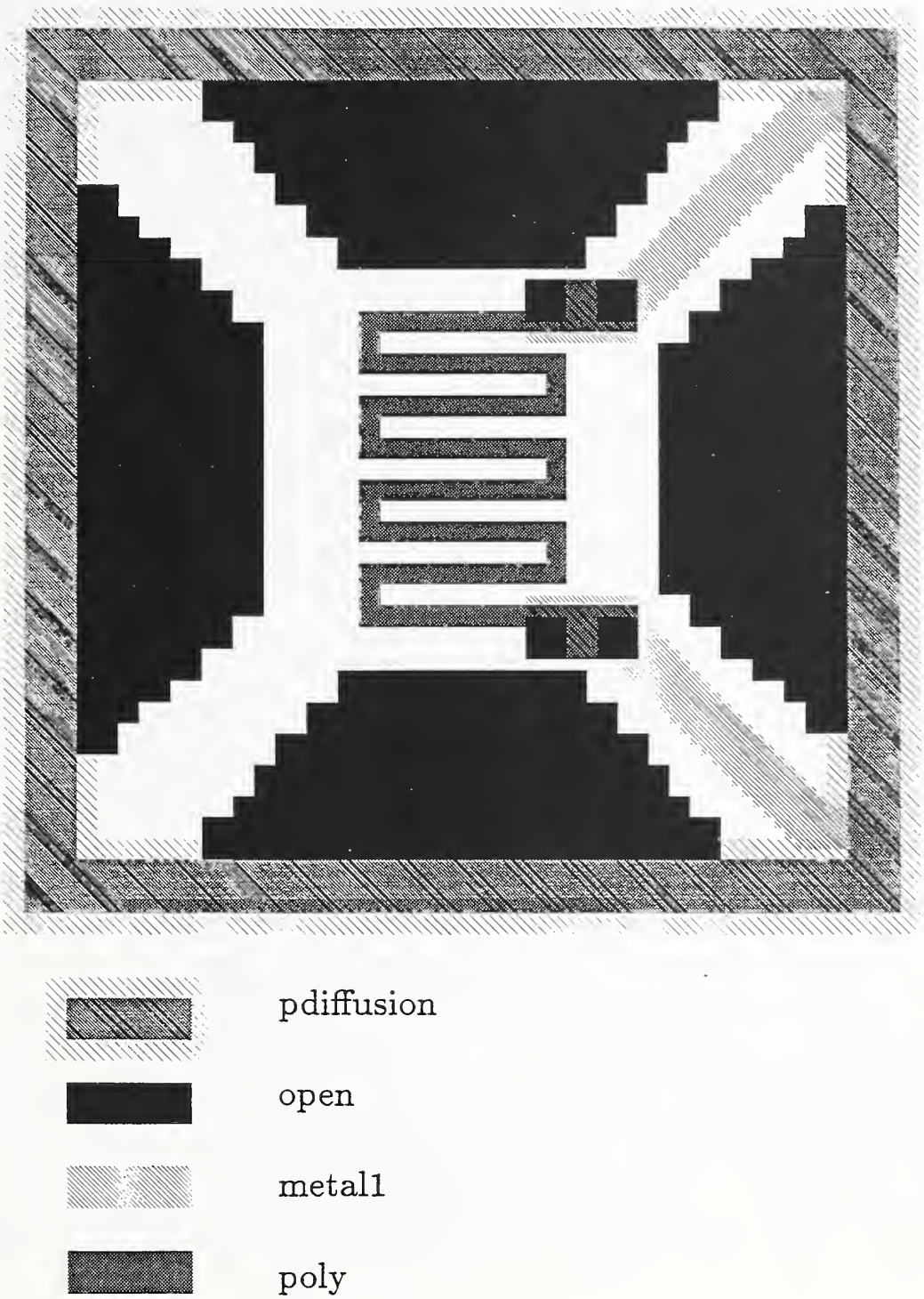


Figure 8. The design of a pixel structure that is used as an infrared point source.

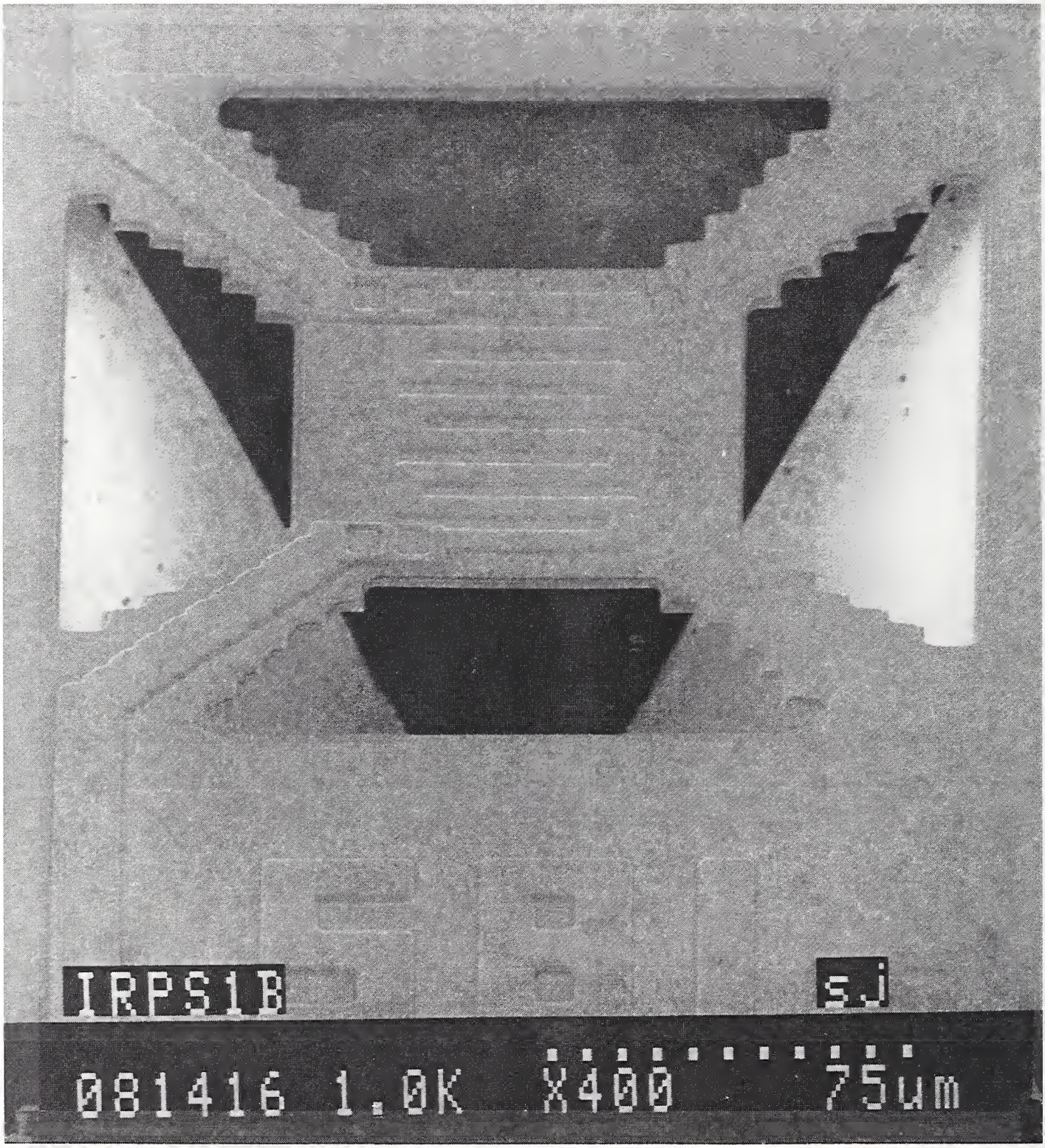


Figure 9. A photomicrograph of the pixel taken after the etch.

Figure 10. A picture of the device operating at incandescence.

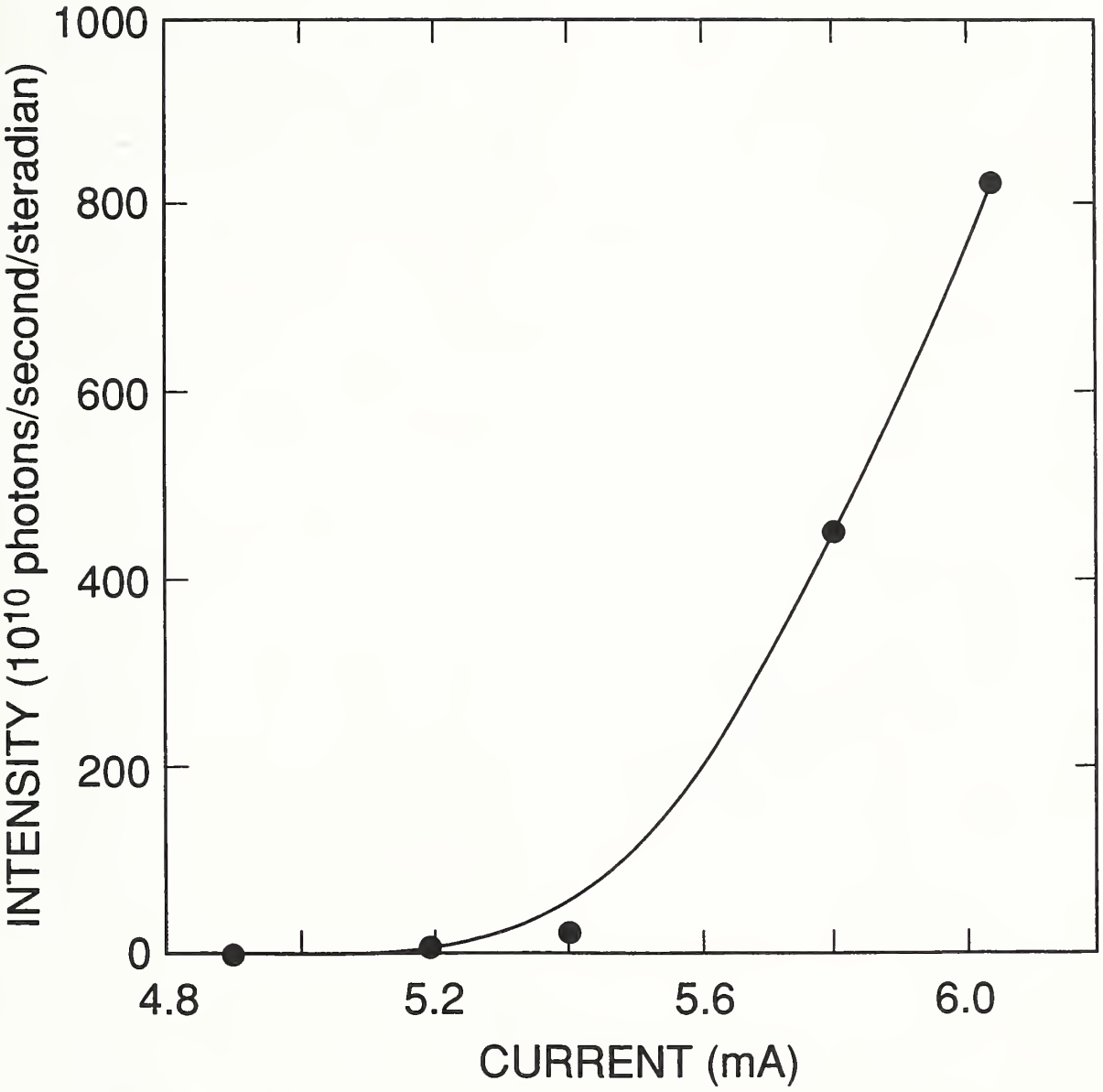


Figure 11. A plot of radiative intensity versus drive current.

Appendix

The Main Features of the Scalable CMOS Micromachine (SCM) Technology File

```
tech
    scm
end

planes
    oxide,ox
    metal2,m2
    metal1,m1
    active,diffusion,polysilicon,act
    well,w
    open
    labelb
end

types /* tiles */

    /* primary layers */

    well bondpad
    metal2 pad
    oxide glass
    metal2 metal2,m2,purple
    metal1 metal1,m1,blue
    active polysilicon,red,poly,p
    active ndiffusion,green,ndiff
    active pdiffusion,brown,pdiff
    active nndiff
    active ppdiff
    well nwell,nw
    well pwell,pw
    open open

    open legend
    labelb legb,legend_background

    /* Contacts between interconnection layers */

    metal1 m2contact,m2c,via,v
    active polycontact,pcontact,pc
```

```
    active ndcontact,ndc
    active pdcontact,pdc
    active nwc,nwcontact
    active pwc,pwcontact

    /* Transistors */

    active ntransistor,nfet
    active ptransistor,pfet

end

contact /* contacts between planes */
    pad metal2 metal1
    m2c metal2 metal1
    pc poly metal1
    ndc ndiff metal1
    pdc pdiff metal1
    nwc nndiff metal1
    pwc ppdiff metal1
end

styles /* colors */
    styletype mos

    poly 1
    ndiff 2
    pdiff 4
    nfet 6
    nfet 7
    pfet 8
    pfet 9
    metal1 20
    metal2 21
    pc 1
    pc 20
    pc 32
    ndc 2
    ndc 20
    ndc 32
    pdc 4
    pdc 20
    pdc 32
    m2c 20
```

```
    m2c 21
    m2c 33
    pwc 5
    pwc 20
    pwc 32
    nwc 3
    nwc 20
    nwc 32
    ppdiff 5
    nndiff 3
    nwell 12
    pwell 13

/*  pad 20
    pad 21
*/
    pad 32

    glass 34

    open 33

    legend 1
    legb 32
    bondpad 32

    error_p 42
    error_s 42
    error_ps 42
end

compose /* to create structures in same plane */
    compose nfet poly ndiff
    compose pfet poly pdiff

    erase glass metal1 space
    erase glass metal2 space

end

#define allMetal2 m2,m2c/m2,pad/m2
#define allMetal1 m1,m2c/m1,pc/m1,ndc/m1,pdc/m1,pwc/m1,nwc/m1,pad/m1
#define allPoly poly,pc/active,nfet,pfet
#define allDiff0 pwc/active,nwc/active,ppdiff,nndiff
```

```
#define allDiff allDiff0,ndiff,pdiff,ndc/active,pdc/active,pfet,nfet
#define allNwell nwell,nwc/active
#define allPwell pwell,pwc/active

cifoutput

style lambda=1.0(gen)
    scalefactor 100
    layer CWN allNwell
    layer CWP allPwell
    layer CMS allMetal2
    layer CMF allMetal1
    layer CPG allPoly
    layer CAA allDiff,open
    layer CVA pad,m2c,open
    layer CCA ndc,pdc,nwc,pwc,open
    layer CCP pc
    layer CSN
bloat-or ndiff,nfet,ndc/active * 200
bloat-or nwc/active,nndiff * 200
grow 100
shrink 100
    layer CSP
bloat-or pdiff,pfet,pdc/active * 200
bloat-or pwc/active,ppdiff * 200
grow 100
shrink 100
    layer COG pad,glass,open

end

cifinput

style lambda=1.0(gen)
    scalefactor 100
    layer nw CWN
    layer pw CWP
    layer m2 CMS
    layer m1 CMF
    layer poly CPG
    layer pdiff CSP
and CAA
    layer ndiff CSN
and CAA
```

```
    layer nndiff CWN
and CSN
and CAA
    layer ppdiff CWP
and CSP
and CAA
    layer nfet CPG
and CAA
and CSN
    layer pfet CAA
and CPG
and CSP
    layer ndc CCA
and CAA
and CSN
and CMF
    layer pdc CCA
and CAA
and CSP
and CMF
    layer nwc CCA
and CAA
and CSN
and CWN
and CMF
    layer pwc CCA
and CAA
and CSP
and CWP
and CMF
    layer m2c CVA
and CMS
and CMF
    layer pc CCP
and CPG
and CMF
    layer pad CMF
and CMS
and CVA
and COG
    layer glass COG
and-not CVA
    layer open CAA
and CCA
```

```
and CVA
and COG

end

drc
    spacing open open 20 touching_ok \
"Open spacing must be at least 20 (Our rule #0.1)"

end
```

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The methodology for implementing the design of silicon-micromachined devices in a standard CMOS foundry process is discussed, and a modified Magic technology file is introduced. The modified technology file is used to design silicon-micromachined devices and circuits that are fabricated using a standard CMOS foundry through the MOSIS service. An additional maskless etch in EDP is required to realize the micromechanical structures once chips are delivered. The modified technology file implements a layer that we call "open" that consists of a combination of active area, contact cut, via, and glass opening. This open area exposes the silicon surface for an anisotropic etch procedure that creates suspended bridges of polysilicon or metal encapsulated in SiO_2. Results from fabricated chips are included.

12. KEY WORDS (6 TO 12 ENTRIES; ALPHABETICAL ORDER; CAPITALIZE ONLY PROPER NAMES; AND SEPARATE KEY WORDS BY SEMICOLONS)

CAD; CIF; CMOS; EDP etch; Magic; micromachining; MOSIS; open area; pixel; technology file

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